IN THE DRAWINGS:

Please substitute the enclosed Figures 1-2 for the original Figures 1-2, which were previously submitted in the application.

IN THE SPECIFICATION:

Please amend the specification as follows:

[0048] More specifically, in Figure 4, item ~~40~~ 400 represents a logical device having x and y inputs and a z output. Once again v represents the victim wire. The victim window v(z) might be the time at which a critical transition could be propagating along V, or might be a time at which the results of a noise-induced erroneous value on v could be stored into a memory element. Unlike Figure 1, in Figure 4, the logic device is provided with a delay (max 4, min 2). In conventional single window analysis this delay causes the beginning of the x switching window to be shifted 2 time units (from 2 to 4) to form the beginning of the z switching window and causes the end of the y switching window to be shifted 4 time units (from 15 to 19) to form the end of the z switching window. In this case the z single switching window is overly pessimistic.